

MICROPROCESSOR INTERFACE

Abstract of the Disclosure

5 A microprocessor interface having: (i) a data
rebuffering section adapted to couple data from a one of a
plurality of data ports to a data port of the microprocessor
selectively in accordance with a control signal; and (ii) a
main memory interface adapted for coupling to a main memory
for the microprocessor, such main memory interface being
coupled to the data rebuffering section for providing
10 control signals to the main memory section for enabling data
transfer between the main memory and the microprocessor
through the data rebuffering section. The main memory is a
selected one of a plurality of memory types each type having
a different data transfer protocol and the main memory
15 interface is configured in accordance with the selected one
of the plurality of memory types to provide a proper memory
protocol to data being transferred between the
microprocessor and the main memory through the main memory
interface. One main memory type is an SDRAM or a RDRAM.